Claim 1

Claim 1 is directed to a circuit comprising a set of interconnected delay stages and switch-controlled load circuitry connected to the output of one or more delay stages. The switch-controlled load circuitry substantially shields the delay stages from noise in a power supply connected to the switch-controlled load circuitry.

Fig. 2 shows an exemplary embodiment of the circuit of claim 1, in which delay stages 202a-c are an example of the set of interconnected delay stages of claim 1, and transistor 204an, switch 206an, and current source 208an are an example of the switch-controlled load circuitry of claim 1. As seen in Fig. 2 and as described in the corresponding text in the specification, the configuration of elements 204an, 206an, and 208an of Fig. 2 substantially shields delay stage 202b from noise in either power supply vdd, which is connected to current source 208an, or power supply vss, which is connected to transistor 204an. In particular, noise in power supply vdd would substantially pass through current source 208an and transistor 204an to power supply vss without reaching delay stage 202b. Similarly, noise in power supply vss would substantially pass through transistor 204an and current source 208an to power supply vdd without reaching delay stage 202b.

Tran does not teach or even suggest circuitry that provides the function explicitly recited in claim 1. In particular, the circuitry taught in Tran does not substantially shield delay stages from noise in a power supply connected to switch-control load circuitry.

Tran teaches an oscillator, such as a voltage-controlled oscillator (VCO), that has circuitry designed to reduce jitter. Significantly, the jitter addressed by Tran is different from the jitter addressed by the present invention. The present invention addresses jitter that results from noise in a power supply, while Tran addresses jitter that results from a threshold band where the input voltage is applied to the control transistors in Tran's delay stages. See, e.g., Figs. 3a-b and column 1, lines 45-54.

Even more importantly, the jitter-control circuitry taught in Tran does not substantially shield Tran's delay stages from noise in Tran's power supplies connected to Tran's jitter-control circuitry.

Tran's Fig. 1a shows the circuit elements of his basic delay stage, as represented symbolically in Fig. 1b. Fig. 2 shows a "prior art" VCO comprising a set of three of these delay stages interconnected with three charging capacitors. Fig. 9 shows an exemplary VCO of Tran's invention comprising three interconnected sets of circuitry, where each set of circuitry includes the basic delay stage of Fig. 1a (albeit with a variable current source) as well as Tran's "jitter-control circuitry," which consists of an inline transistor (see 24 of Fig. 4) and a pull-UP/DOWN output transistor (see 25 of Fig. 4).

As is clear from Figs. 4, 7b, and 9, any noise in power supply V_{DD} will substantially pass through the current source and the inline transistor and be applied to the next delay stage via V_{out}. Thus, the jitter-control circuitry of Tran does not substantially shield Tran's delay stages from noise in Tran's power supplies connected to Tran's jitter-control circuitry.

For all these reasons, the Applicant submits that claim 1 is allowable over Tran. Since claims 2-17 depend variously from claim 1, it is further submitted that those claims are also allowable over Tran.

Claim 3

According to claim 3, the switch-controlled load circuitry selectively applies a load to the corresponding delay stage output. Tran's jitter-control circuitry consists of an inline transistor (e.g., 24 of

Fig. 4) and a pull-UP/DOWN output transistor (e.g., 25 of Fig. 4). In order for Tran's jitter-control circuitry to be an example of the switch-controlled load circuitry of claim 3, then transistor 24 would have to be the switch of claim 3 and transistor 25 would have to be the load of claim 3. But transistor 24 does not "selectively apply" the load of transistor 25 to the output of the corresponding delay stage. In fact, in Tran's disclosed configuration, any load from transistor 25 is always applied to the output of the corresponding delay stage, independent of the state of transistor 24. Thus, Tran does not teach switch-controlled load circuitry that selectively applies a load to the corresponding delay stage output. The Applicant submits that this provides additional reasons for the allowability of claim 3 (and therefore also claim 4) over Tran.

Claim 7

According to claim 7, for each delay stage output, the switch-controlled load circuitry (1) is connected between the power supply and the delay stage output and (2) comprises a current source, a load, and a switch, wherein the switch is adapted to selectively apply the load to the delay stage output. Based on reasoning similar to that given previously for claim 3, the Applicant submits that this provides additional reasons for the allowability of claim 7 (and therefore also claims 8-16) over Tran.

In view of the foregoing, the Applicant submits that the rejections of claims under Sections 102(b) and 103(a) have been overcome.

In view of the above remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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